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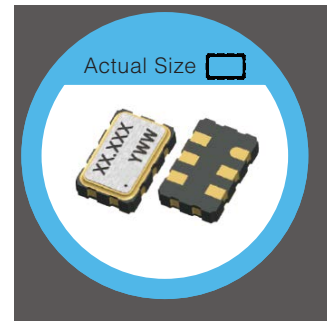
5.0 x 3.2 mm SMD LVPECL/LVDS/ HCSL Crystal Oscillator

FEATURE

- Typical 5.0 x 3.2 x 1.25 mm hermetically sealed ceramic package.
- Very low jitter performance: typical 0.3 pS RMS from 12 k - 20 MHz.
- Fundamental/3rd overtone crystal design.
- Output frequency up to 320 MHz.
- Operating temperature up to 125°C
- Tri-state enable/disable

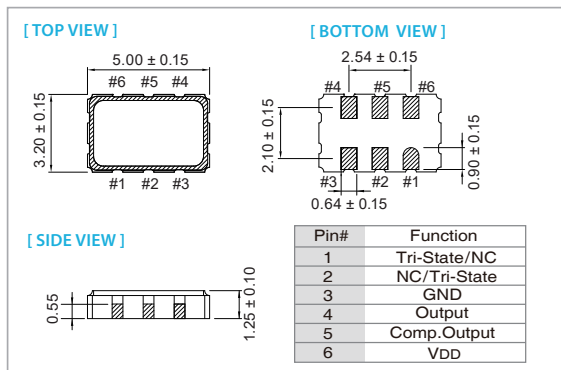
TYPICAL APPLICATION

- 10Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

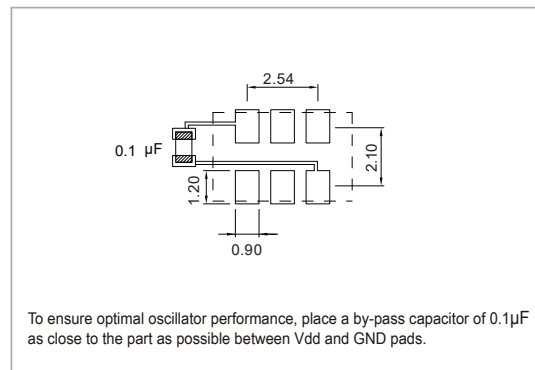


RoHS Compliant

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



ELECTRICAL SPECIFICATION

Parameter	LVPECL				LVDS				unit
	3.3 V		2.5 V		3.3 V		2.5 V		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (V _{DD})	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range	10	320	10	320	10	320	10	320	MHz
Standard Frequency	25, 106.25, 125, 156.25, 161.1328, 212.5								MHz
Supply Current	10 MHz ≤ Fo < 160 MHz		75		75		50		mA
	160 MHz ≤ Fo < 250 MHz		100		100		50		
	250 MHz ≤ Fo < 320 MHz		100		100		65		
Output Level	Output High		2.275		1.475		-		V
	Output Low		-		1.68		0.88		
Transition Time: Rise/Fall Time ⁺	-		1.0		-		1.0		nSec
Start Time	-		10		-		10		mSec
Tri-State(Input to Pin 2 or Pin 1)									
Enable (High voltage or floating)	2.31		-		1.75		-		V
Disable (Low voltage or GND)	-		0.99		-		0.75		
RMS Phase Jitter (Integrated 12 KHz - 20 MHz)									
Fo < 80 MHz	-		1		-		1		pSec
80 MHz ≤ Fo < 125 MHz	-		0.5		-		0.5		
125 MHz ≤ Fo < 170 MHz	-		0.3		-		0.3		
170 MHz ≤ Fo < 200 MHz	-		0.5		-		0.5		
200 MHz ≤ Fo	-		0.3		-		0.3		
Phase Noise@ 156.25 MHz	100 Hz		-95		-90		-90		dBc/Hz
	1 kHz		-125		-125		-120		
	10 kHz		-140		-140		-140		
Aging (@ 25°C 1st year)	-		±3		-		±3		ppm
Storage Temp. Range	-55		125		-55		125		°C

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

Parameter	HCSL				unit
	3.3 V		2.5 V		
	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range	25	175	25	175	MHz
Standard Frequency	100				
Supply Current					
25 MHz ≤ Fo ≤ 175 MHz	–	50	–	50	mA
Output Level					
Output High	0.6	–	0.58	–	V
Output Low	–	0.15	–	0.15	
Transition Time: Rise/Fall Time+	–	0.5	–	0.5	nSec
Start Time	–	10	–	10	mSec
Tri-State(Input to Pin 2 or Pin 1)					
Enable	0.7VDD	–	0.7VDD	–	V
Disable	–	0.3VDD	–	0.3VDD	
RMS Phase Jitter (Integrated 12 kHz ~ 20 MHz)					
25MHz ≤ Fo ≤ 175MHz	–	0.5	–	0.5	pSec
Aging	–	±3	–	±3	ppm
Storage Temp. Range	-55	125	-55	125	°C

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	ppm	±25	±50
-10 ~ +60		○	○
-20 ~ +70		○	○
-40 ~ +85		△	○
-40 ~ +125		×	○

* ○ : Available △:Conditional X: Not available

* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.